Customer No.: 31561
Docket No.: 9289-US-PA
Application No.: 10/065,342

In the Specification

Please amend the paragraphs [0006] and [0022] as follows.

[0006] At present, most DDR DRAM modules in the market use a 184-lead memory module slot that meets the JEDEC standard while the SDRAM modules use a 168-lead memory module slot. Hence, a memory module must be fabricated according to the memory slot standard and the final product must be tested before shipment. Fig. 1 is a flow chart showing the steps for fabricating a conventional memory module. The fabrication starts out with the input of a memory chip (S110). Subsequent processes include assembling (S120), testing (S130). If nothing goes wrong after a testing operation (S150), the product is ready for shipment. On the other hand, if failure is found in some memory address (S140), the failed memory chip is manually de-soldered (S160) and replaced with a new one. Another test is carried out to confirm the repaired memory module is error free.

[0022] Fig. 2 is a flow chart showing the steps for fabricating a memory module according to one preferred embodiment of this invention. As shown in Fig. 2, the fabrication of a memory module starts out with the input of a memory chip (S210). This is followed by assembling (S220) [[~~and~~]], testing (S230) and determining if any failure is found (S240). If the assembled memory module passes the test, the memory module is ready for shipment (S250). On the other hand, if the memory module fails the test, the faulty memory addresses are replaced by standby memory addresses of memory cells within the memory chip. In other words, the

memory module testing/repairing procedure according to this invention is adopted instead of replacing the faulty memory chip manually so that production time and cost are saved.